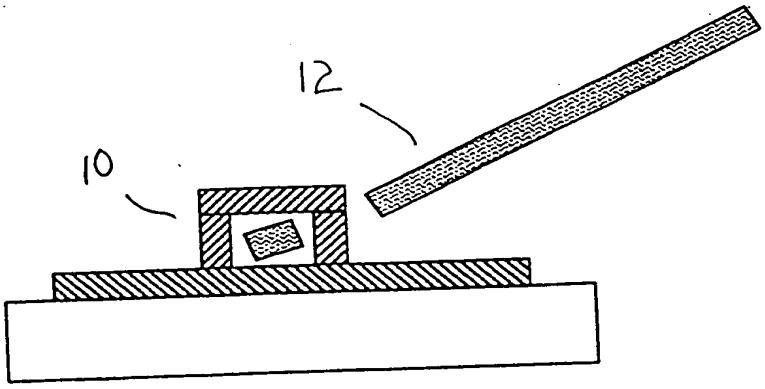


FIGURE 1

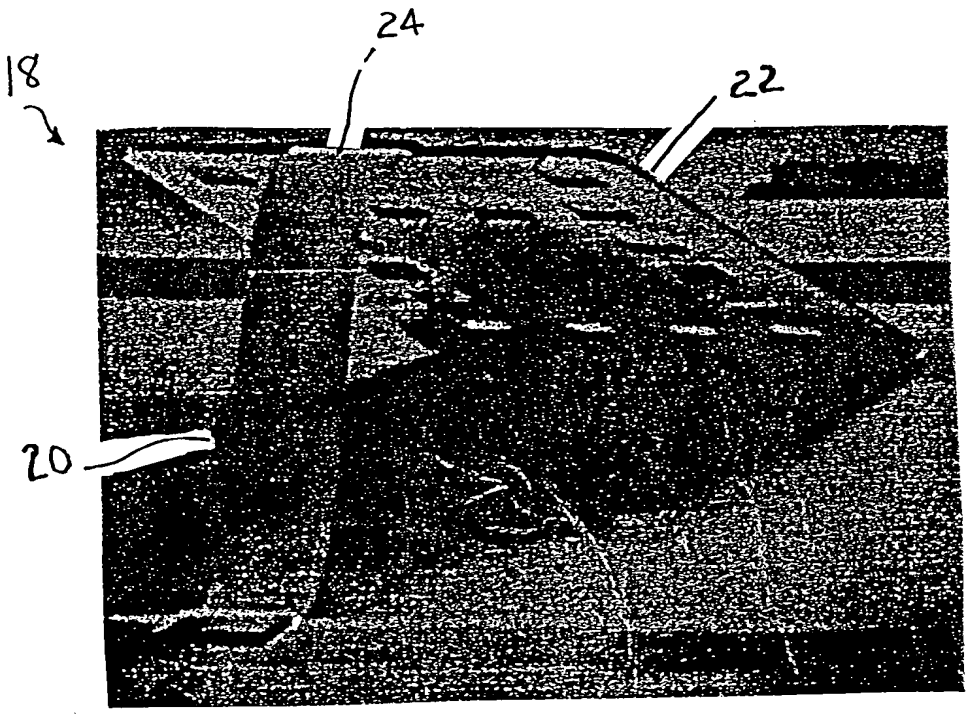


FIGURE 2

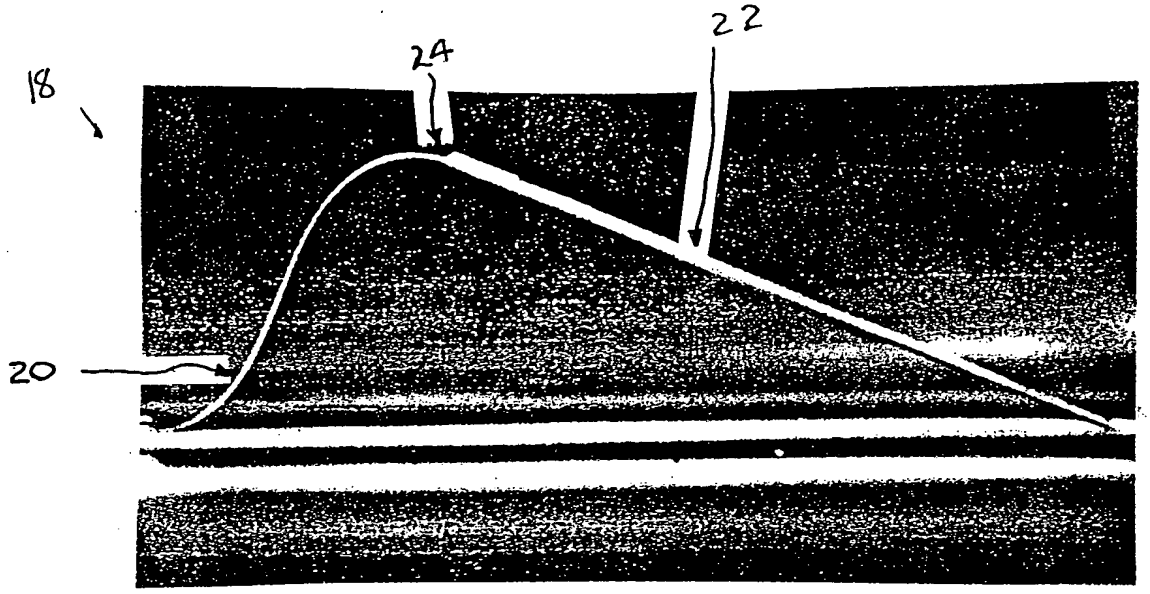
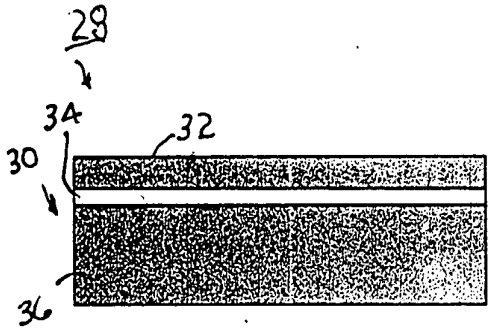
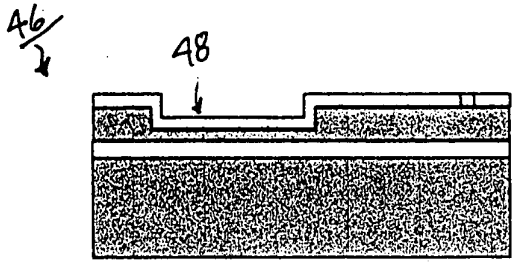


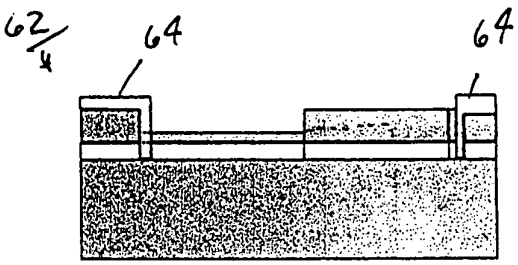
FIGURE 3



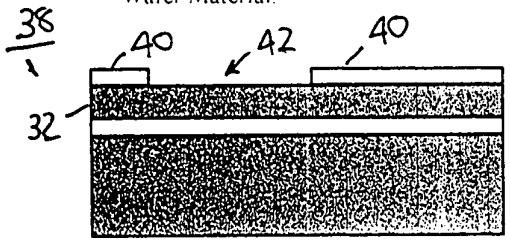
Start with cleaned SOI (Silicon On Insulator) Wafer Material.



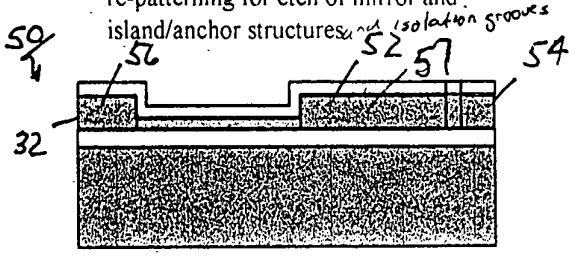
Remove previous resist layer before re-patterning for etch of mirror and island/anchor structures.



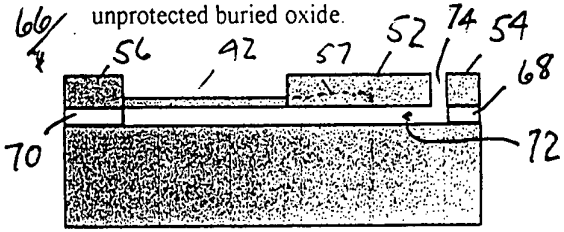
Deposit and pattern final photoresist layer for use during buried oxide release. Release device by etching all unprotected buried oxide.



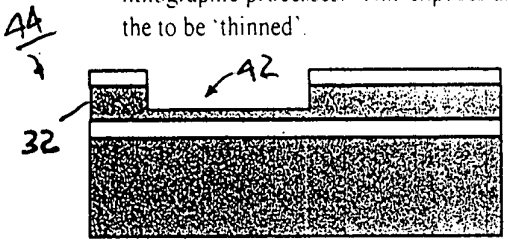
Deposit photoresist and pattern using std lithographic processes. This exposes area the to be 'thinned'.



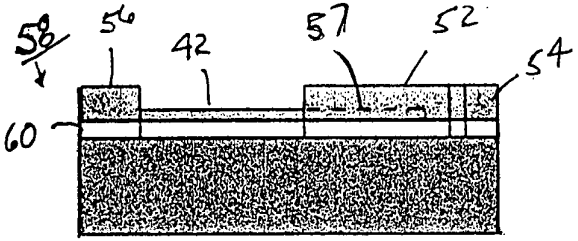
Dry etch exposed silicon to form device structure.



Remove all remaining photoresist in dry O_2 plasma etch process.



Wet etch (KOH 45% @ 60°C) exposed device layer silicon to a thickness of ~500nm.



Remove photoresist and begin etching exposed buried oxide layer (using HF 49%).

FIGURE 4

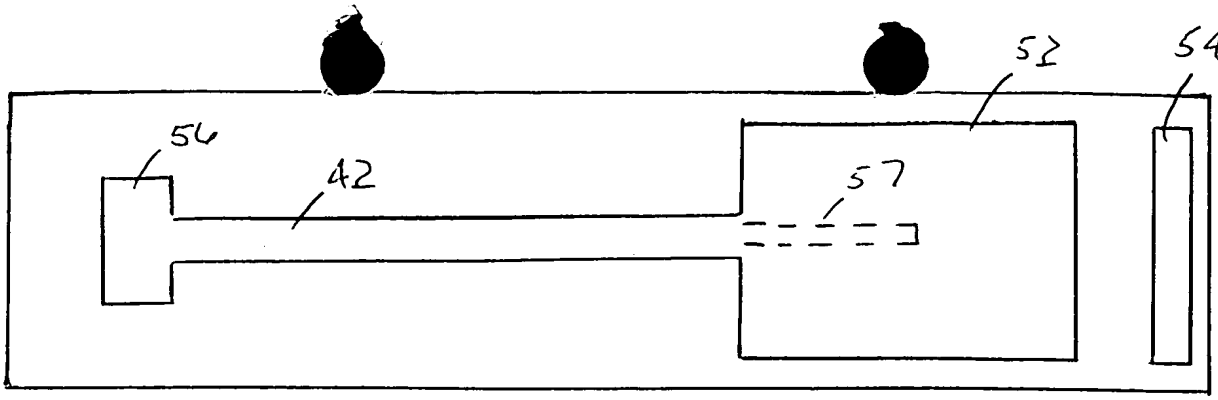


FIGURE 5

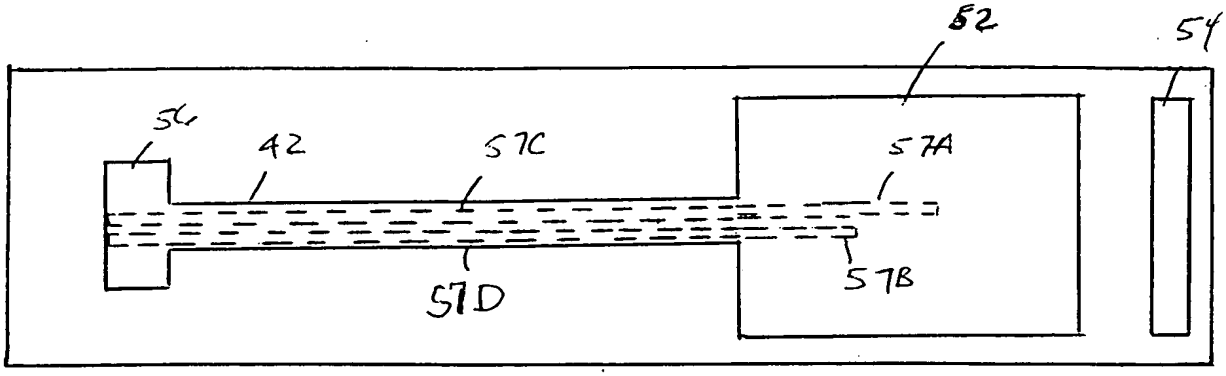


FIGURE 6

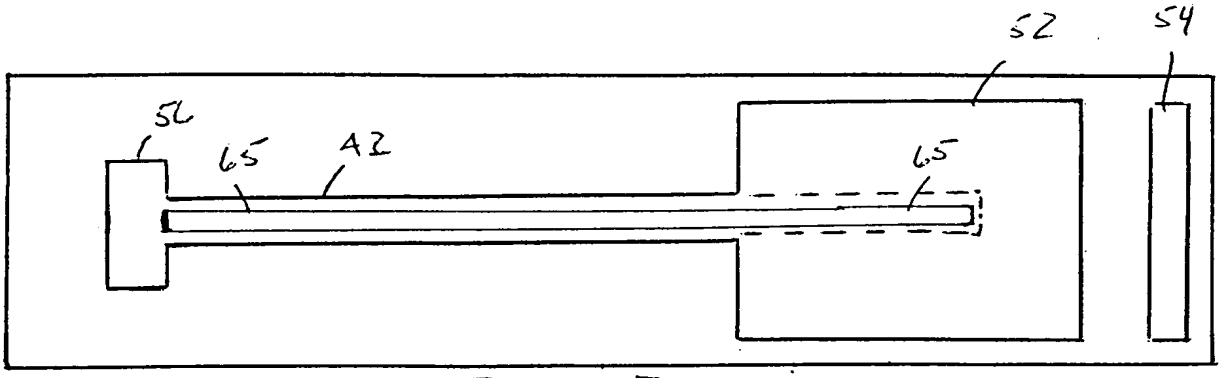


FIGURE 7

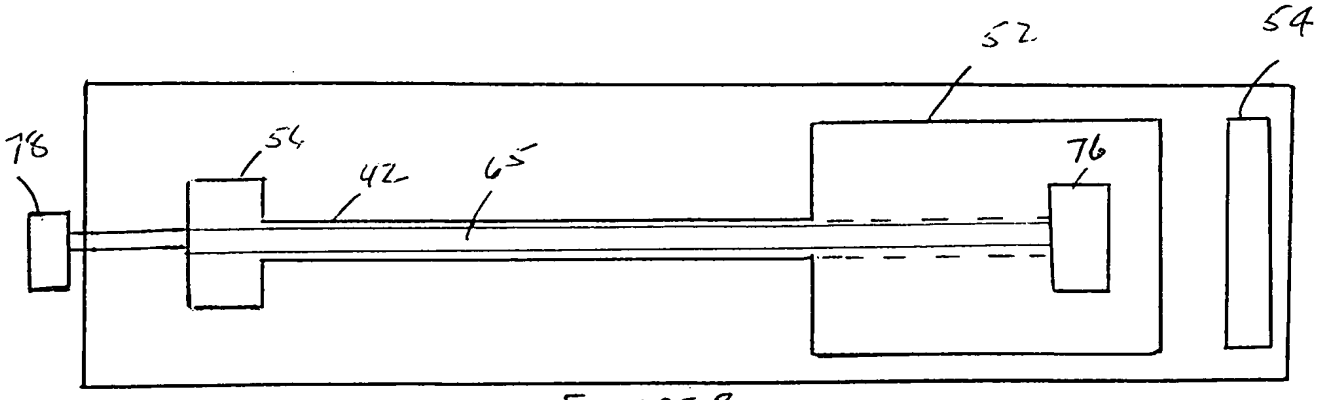


FIGURE 8